Quarterly report
Chronic Microelectrode Recording Array
NIH/NINDS
Period 01/01/05 – 03/31/05

Project: NIH/NINDS **Contract-No.** HHSN265200423621C
Date: 01/01/05-03/31/05

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I. Executive summary

The overall goal of the contract No. NIH/NINDS HHSN265200423621C is to develop and test (in-vivo) a chronically implantable neural recording array and provide the device to the neuroscience community upon completion of the initial technical development phase for experimental use and evaluation.

The objective of the second quarter (Q2) as proposed was to:

a) Re-establish a stable process for fabrication of Utah Electrode Arrays (UEA) and improvement of backplate thinning process and fabrication and characterization of handling tool for transportation and flip-chip bonding
b) Install equipment and processes for Parylene and SiC coating procured in the 1st quarter
c) Design and simulation of signal processor module, initiation of 1st generation chip MOSIS production run
d) Design and simulation of LTCC based coils, characterization of test coils for final design specification
e) Further development of flip-chip bonding technology (test structures and characterization)
f) Further development of Parylene and SiC coating processes, materials characterization (material composition, electrical and chemical properties)

Throughout the second quarter, all the above mentioned objectives (a-f) were accomplished. The results obtained in this quarter further support the validity of the proposed device design and fabrication approach.

Talks were commenced with potential additional collaborators in the field (FES Center, Case Western Reserve University, Innersea Ltd.) in order to improve information exchange between device users and technology providers (materials / biocompatibility). In order to foster progress and accomplishment of the engineering goals, an invitation was accepted for a meeting with researchers at the University of Michigan WIMS Center is planned for June/July 2005. Furthermore, we have initiated an Integrated Neural Interface Program (INIP) Meeting for a) all researchers involved in neuroprosthetics research at the University of Utah and b) interested external parties from the general research community. The first INIP meeting is scheduled for April 21st 2005.

II. Activity Summary

Key results for project period (Q II) (work packages)

- Fabrication of ultra thin Utah Electrode Array and supplemental MEMS tools: fabrication and thermal characterization of a handling tool for transportation and flip-chip bonding; fabrication of UEAs
- Development and fabrication of electronics and communications module: simulation of CMOS signal processor design including forward and reverse telemetry module, power recovery module, A/D converter, multiplexer, spike detector and amplifier; initiation of MOSIS fabrication of 1st generation chip
- Development and fabrication of LTCC ferrite coil: simulation and optimization of coil design/geometry based on initial test results leading to final design
- Flip-chip bonding and assembly: fabrication of additional flip-chip test structures emulating UEA and signal processor modules for metallization, bonding process and underfiller optimization, start of bond metallization adhesion and wetting properties on UEA and signal processor base metallization
- Hermetic encapsulation and layer coating: installation of Parylene CVD coater, fabrication of test structures for coating layer adhesion and electrical characterization (acute and long-term), deposition of silicon carbide and parylene layers on test structures, characterization of layer composition, start of electrical testing of layers in saline/buffer solution

Meetings/presentations during project period (Q II)

- Invited talk on wireless chronically implantable neural recording array at FES Center, Case Western Reserve University, Cleveland, OH, March 25th 2005. Meetings and discussions with Bob Kirsch, Hunter Peckham, Dominique Durand, Dawn Tayler, Dustin Tyler and various technicians.
- Telephone conferences with IBMT and IZM
- Individual weekly project meetings of the project teams at the University of Utah as well as the subcontractors; meeting minutes are created in common format by all partners.

Patents (Q II)

- No additional new invention disclosures, further processing of previously submitted invention disclosures

Organizational accomplishments (Q II)

- Employment of new technician
- Signing of subcontracts (not signed, yet)
- Organization of INIP meeting, Logo development for INIP program

III. Research Results and Discussion

III.a. Probe system fabrication

III.a.1 Task 1 Fabrication of ultra thin Utah Electrode Array

Description/Rationale

Conventional Utah Electrode Arrays were built for a variety of testing purposes. Optimization of the backplate thinning process has begun. No further activities were planned for the second quarter.

Future plans for the next two (2) quarters

In the coming two quarters, the polishing process will be finalized for electrode arrays with thinned backplate, including characterization.

III.a.2 Task 2: Development and fabrication of electronics and communications module

Description/Rationale

The electronics/communication module will be a single CMOS integrated circuit mounted on the back of the microelectrode array. Two or three surface-mount capacitors mounted near the chip to provide capacitance values not achievable on chip are planned. The electronics module will amplify and process neural signals, transmit this data out of the body on an RF carrier, and receive power and command data from the power coil via a transcutaneous magnetic link.

Experimental Results

We have completed simulation and layout for our first integrated circuit: Integrated Neural Interface chip version 1.0 (INI1). The chip was submitted to MOSIS for fabrication on 11 March 2005. We expect to receive silicon (40 copies) in late May or early June. The chip will measure approximately 4.7 mm × 5.9 mm. Twelve of the returned chips will be packaged in small, 52-pin ceramic packages to facility bench-top testing in Harrison's lab. The remaining 28 chips will be used for flip-chip bonding tests.

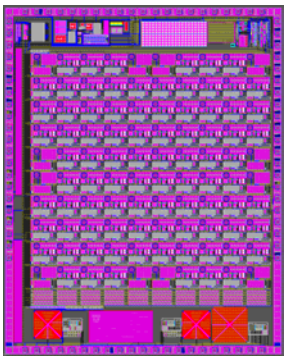

Fig. 1: Layout of Integrated Neural Interface chip version 1.0 (INI1) The fabricated chip will measure 4.7 mm × 5.9 mm and contain over 30,000 transistors and over 5,000 passive components (capacitors, resistors, inductors, and diodes).

- **Power recovery module.** This module interfaces with the power coil and converts the unregulated ac voltage on the coil into a regulated dc voltage to power the chip. We use an on-chip full-wave bridge rectifier to convert ac to dc. A linear voltage regulator with a bandgap voltage reference is used to regulate the power supply voltage at 3.3 VDC. The ac power signal will be operating at 2.64 MHz.
- **Forward telemetry module.** This module also interfaces with the power coil and performs two functions. First, this circuit generates a stable, digital (square wave) 330-kHz clock synchronized to the oscillation on the coil (divided by eight). This clock serves as a frequency reference for the entire chip. Second, this circuit identifies changes in the amplitude of the ac voltage waveform on the coil. These amplitude changes will be used to send telemetry data (e.g., configuration commands) to the implanted device. The circuit interprets each amplitude change as a 'one' or 'zero' based on the

length of each pulse, and loads this binary data stream into on-chip configuration and command registers. Our current chip has 128 bits of internal configuration bits.

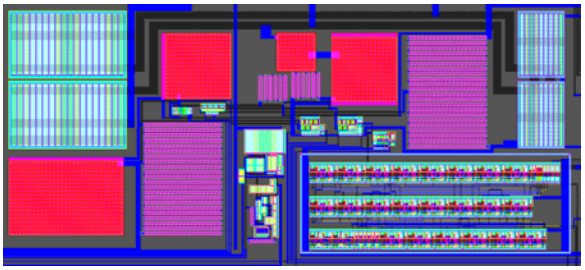

Fig. 2: Detail of INI1 chip layout showing power recovery and forward telemetry interface circuitry. On-chip diodes rectify the ac power received by the coil, and a digital controller extracts amplitude-modulated data from the power waveform.

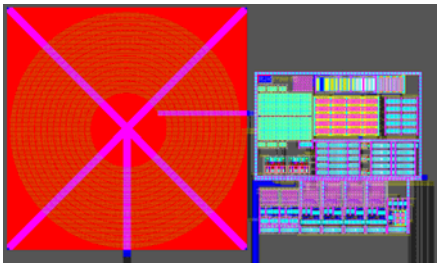

Fig. 3: Detail of INI1 chip layout showing fully-integrated 433-MHz data transmitter. The on-chip planar spiral inductor measures 500 μm in diameter and acts as transmitting antenna.

- **Neural signal amplifiers and spike detectors.** A 10 × 10 array of neural signal amplifiers and spike detector circuits form a 4 mm × 4 mm array at the center of the chip. Each amplifier has an octagonal bond pad 70 μm in diameter that will connect to the microelectrode array. Each amplifier has a gain of 60 dB and a bandwidth from 300 Hz (to block large-amplitude local field potentials) to 5 kHz. A comparator is used to detect spikes by comparing the output of the neural amplifier to a programmable reference level set by an on-chip digital-to-analog converter (DAC).

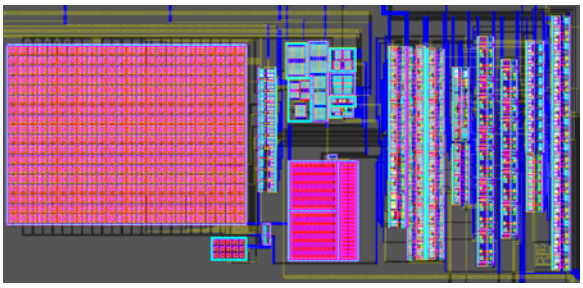

Fig. 4: Detail of INI1 chip layout showing fully-integrated 10-bit analog-to-digital converter (ADC) designed. The circuit utilizes a large capacitor array (left) to implement a low-power charge redistribution architecture.

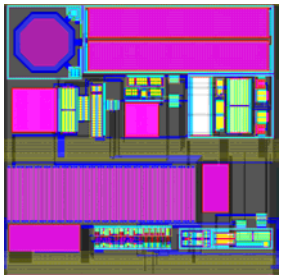

Fig. 5: Detail of INI1 chip layout showing a single neural amplifier cell. The amplifier has a gain of 60 dB and a bandwidth of 300 Hz – 5 kHz. Each cell includes a spike detector for data reduction. The 70-μm octagonal bondpad in the upper left corner contacts the UEA.

- **Analog-to-Digital Converter.** The chip has a 10-bit analog-to-digital converter (ADC) to digitize a selected neural waveform at 15 kSamples/s. An analog multiplexer (MUX) is used to route the selected neural amplifier signal to the ADC.

- **RF transmitter for reverse telemetry.** An on-chip RF transmitter transmits the digital data from the ADC and the spike detectors. The transmitter operates in the 433 MHz ISM band at a rate of 330 kbit/s using binary amplitude-shift keying (ASK) and/or frequency-shift keying (FSK). Optimized on-chip planar spiral inductors will minimize power consumption. Recent successes with on-chip inductor optimization suggest that an off-chip inductor will no longer be necessary.

Discussion/Interpretation of Results

Simulations show that the INI chip architecture as implemented should allow for a fully-functional integrated neural interface. However, we have made the initial design modular so that each component can be tested separately. This will allow us to work around any subcircuits that do not work as expected in the bench-top tests, and determine the cause of failure so that it can be corrected in version 2 of the chip. Initial tests of a previously integrated charge-redistribution ADC show an integral nonlinearity error

(INL) of ±6 LSB over a range of 0.7 V – 3.2 V when powered from a 3.3 V supply. We have submitted a revised version of the ADC for fabrication which should have lower INL error. Simulations indicate that the ADC module will consume less than 7 µW of power.

Future Plans for Next Two (2) Quarters

The INI1 chip is currently being fabricated through MOSIS in AMI Semiconductor's 0.5-µm 2-poly, 3-metal CMOS process. We will receive 40 copies of the chip in early June; twelve of these will be packaged in ceramic chip carriers for bench-top testing. The remaining 28 bare die will be used to test the assembly and coating steps. Bench-top testing will commence upon receipt of the packaged chips. After testing the chip, we will begin the design of version 2 in July, which will address any shortcomings found in version 1. Submitted for fabrication is on 6 September 2005, return from fabrication is mid-November.

III.a.3 Task 3: Development and fabrication of LTCC ferrite coil

a. Initial establishment of simulation model

Description/ Rationale

For reliable modelling of the coil, the simulation has to be matched to the experimental results of the test coils. The objective is to determine the optimal design of the power receiving coil and the transmission efficiency. Field simulations were performed using *FlexPDE* version 4.0.1a. Although the coils will be fabricated in square form, all field simulations in this study were performed with 2-D axi-symmetric models (circular coils), in order not to exceed the calculation capacity of the software. Coil geometries and material parameters are given in our 1st quarterly report.

Experimental (Simulation) Results

Simulations show different inductances, smaller resistances, and larger Q's than the measurements. Discrepancies may be caused by the model used (circular coils were used, instead of square coils), the value for the conductivity of screen-printed gold and the dimension shrinkage after firing. Self inductance and Q-factor of the coils were simulated as a function of the number of turns (Fig. 6). $Q_{max.}$ is obtained when coil windings fill 80-85 % of the coil diameter. The self inductance increases with the number of turns.

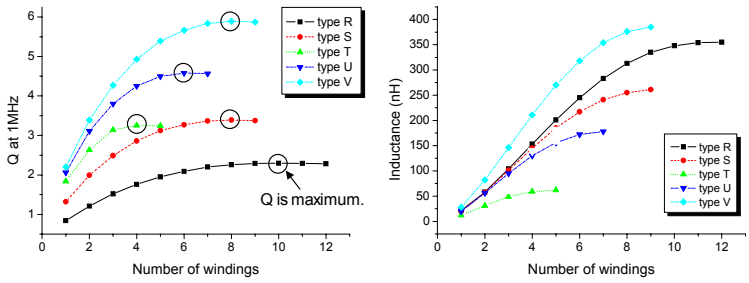

Fig. 6: Simulated Q and L according to the number of windings/turns.

Tab. 1: Simulated characteristics of LTCC coils, compared with measured values.

Coil type	Simulation (circular coil)			Measurement (square coil)		
	L (nH)	R (Ω)	Q at 1MHz	L (nH)	R (Ω)	Q at 1MHz
R	201	0.647	1.95	180	0.74	1.5
S	185	0.373	3.12	160	0.41	2.5
T	49	0.098	3.14	60	0.14	2.7
U	130	0.192	4.25	140	0.25	3.5
V	270	0.315	5.39	240	0.38	4.0

Fig. 7 shows the coupling between two coils, as function of the diameter of the transmitting coil and the coil separation. The diameter of the implanted receiving coil is fixed at 5 mm. The optimum diameter of the transmitting coil is correlated to the separation. With weak coupling (< 0.033), the voltage gain between the transmitting and receiving coils ranges from 1.1-2 and the power efficiency from 7-27 %.

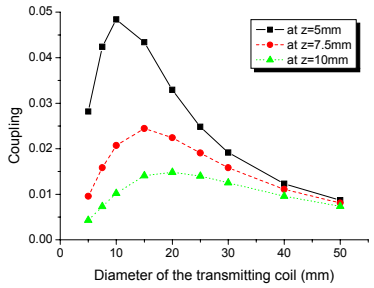

Fig. 7: Coupling between two coils, as a function of the diameter of the transmitting coil and the operating distance z. The diameter of the receiving coil is 5 mm.

Fig. 8: Schematic of a single-layer LTCC coil.

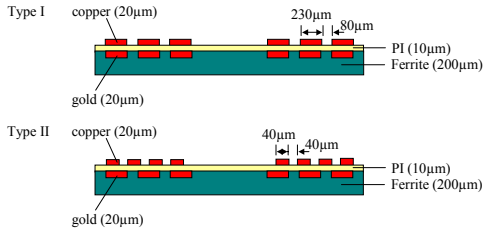

Fig. 9: Two types of a multi-layer coil.

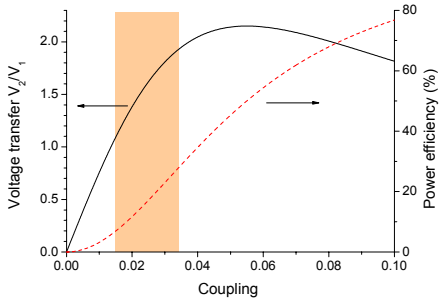

Fig. 10: (Singe layer coil): voltage transfer and power efficiency between two coupled coils (shadowed region: obtainable values for coils). Load resistance: 10 kΩ.

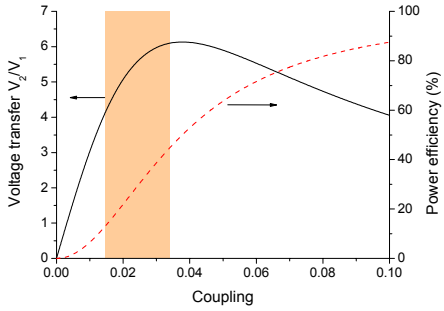

Fig. 11: (Multi-layer coil): voltage transfer and power efficiency between two coupled coils (shadowed region: obtainable values for coils). Load resistance: 10 kΩ.

Discussion / Interpretation of results

For receiving coils, the Q_{max} is obtained when the turns fill the coil diameter by about 80 %, independent of the dimension of the line width and spacing. For transmitting coils, a 2-4 times larger diameter is necessary to get a moderate coupling for an operating distance between coils slightly larger than the diameter of receiving coils. Q of the transmitting coil has to be high enough for a reliable power transmission, but should not be so high as to generate too much heat (danger to patients). For a receiving coil with a diameter of 5 mm and the operating distance of 5-10 mm, a coupling of 1.5-3.3 % is expected. A single-layer coil allows a voltage and power transmission of 2 and 27 % respectively at 5 mm separation, depending on the Q of the transmitting coil. With a multi-layer coil, a voltage amplification of 6 and a power efficiency of 43 % may be obtained at a distance of 5 mm.

b. Test structures and simulation of integrated neural interface coil

Description/Rationale

In the complete neural interface, a small coil will be used to receive the magnetic ac power waveform transmitted through the skin at 2.64 MHz. The coil will measure approximately 5 mm × 5 mm.

Experimental Results

The largest three LTCC coils (S, V, and U) were tested as receivers using a 2.2-cm diameter transmitting coil at a frequency of 2.64 MHz (operating frequency for our IC) with a copper transmitting coil (2.2 cm

in diameter, 17 turns on two layers, inductance of 6.03 μH). A function generator was used to produce a 2.64-MHz 13.8 V peak-peak sine wave across the transmitting coil. In the final device, the voltage will be limited to 100 V_{rms} for safety reasons. The results obtained here can easily be extrapolated to this higher voltage. Each receiving coil was centered 1 cm below the transmitting coil. The voltage on the receiving coil was measured with a 100 kΩ load. The voltages received are insensitive to changes in load so long as it stays well above the series resistance of the receiving coil.

Tab. 2: LTCC Coil Measurements

Coil type	**S**	**V**	**U**
Outside dimensions	4.0 x 4.0 mm	6.0 x 6.0 mm	4.8 x 4.8 mm
Number of turns (N)	5	5	4
Measured inductance (L)	174 nH	261 nH	105 nH
Measured series resistance (R_s)	0.564 Ω	0.405 Ω	0.231 Ω
Q @ 2.64 MHz ($Q = 2\pi fL/R_s$)	5.1	10.7	7.5
Voltage Gain	0.0022	0.0040	0.0006
Inductor coupling coefficient k	0.013	0.019	0.004

Coil V has the highest voltage gain and coupling coefficient. This is expected since V is the largest coil. With a gain of only 0.0040, a 100 V amplitude on the transmit coil would yield only 0.4 V at the receive coil. We have conducted some experiments with capacitors, and thus far we do not observe a voltage increase by a full factor of Q (perhaps due to the ESR of the capacitor). We observed an increase by only $0.3Q$ with the S coil. Also, due to the relatively small value of the coil inductance, we have to use capacitors in the 10 nF range to resonate at 2.64 MHz. In summary, a coil with more inductance (larger area and/or more turns) is likely needed. We would like to see voltages in the 10 V amplitude range on the receiving coil. We have recently completed a preliminary design of a planar spiral coil that could be fabricated with 15-μm thick copper traces on a thin-film substrate. SPICE simulations with an 80-turn inductor of this type yield $L \approx 30$ μH and $R_s \approx 150$ Ω. For 80 turns, the windings would have a width of approximately 13 μm with a wire spacing of 10 μm. At 2.64 MHz, this inductor has a Q factor around 3, and we observe a voltage boost by this factor if we add a ~100 pF capacitor in parallel with the inductor.

Discussion/Interpretation of Results

An inductor somewhere near this point in design space (5.5 mm diameter; 80 turns; $L \approx 30$ μH; $R_s \approx 150$ Ω; $Q \approx 3$ @ 2.64 MHz) will give us an adequate received voltage for a transmit coil voltage of 100 V peak. Simulations show an improvement by over one order of magnitude from the best conventional test coil we tested. The addition of a high-μ ferrite material placed underneath this thin-film coil will (1)double the inductance and Q factor of the coil, which reduces the value of the resonant capacitor by half and boosts the received voltage, (2) shield the coil from the conductive silicon integrated circuit beneath it (assuming a non-conductive ferrite) preventing eddy currents that reduce the effective inductance and increased series resistance and (3) shield the underlying amplifiers and electrodes from the large 2.64-MHz magnetic field. Using the ferrite material, we estimate that the final parameters of the coil would be close to: 5.5 mm diameter; 80 turns; $L \approx 60$ μH; $R_s \approx 150$ Ω; $Q \approx 6$ @ 2.64 MHz. Simulations show that an inductor of this type could receive voltages sufficient for powering the integrated electronics while keeping the voltage on the transmitting coil to less than 100 V_{rms}.

Future Plans for Next Two (2) Quarters

We will coordinate with our colleagues at Fraunhofer IZM on the development and testing of this thin-film power coil. We will also continue development of an efficient class-E power transmitter that will drive the transmitting coil at 2.64 MHz with voltages up to 100 V_{rms}. We will add functionality to this transmitter to facilitate amplitude-modulation of the power waveform for forward telemetry.

III.a.4 Task 4: Flip-chip bonding and assembly (2 pages)

Description/Rationale

Si test wafers were provided by the University of Utah: one with Al pad metallization as test wafer for electroplating and one with Ti/Pt/Au pad metallization for reflow soldering. Experiments were carried out to characterize these metallizations. Thickness measurements of the glass structures on the UEA were performed to get information about the height deviation on chip level. These measurements are useful for the design of the handling tool. Finally a selection of applicable underfiller materials was made.

Experimental Results

IC test chip: A 4" Si wafer with 1.7 µm Al pad metallization was diced. The dies are in use for the testing of the single chip electroplating process. Single chips were arranged in a matrix for AuSn electroplating. Alignment and the bumping were checked. AuSn bumping was selected as the preferred bumping process for this project. In addition, Au stud bumping tests were carried out on the ICs using 25 µm diameter Au wire. Successful bumping on these Al pads was not possible. Since the Al pad metallization on the functional ICs will be processed by MOSIS, this is not expected to be a problem and will not influence the final assembly procedure.

UEA test chips: A Si test wafer with Ti 50 nm/ Pt 240 nm/ Au 200 nm pad metallization was diced. Au80Sn20 solder preforms with diameters in the range of 20 to 30 µm were used to investigate the bondability of the pad metallization. Flux was dispensed on the test chips and the solder preforms were deposited on the surface. A standard AuSn reflow profile was applied. The microscope image (Fig. 12) demonstrates that a good wetting of the bond pads was achieved.

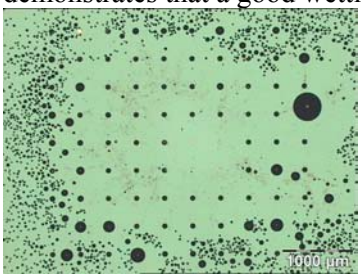

Fig. 12: light microscope image of a test IC with Ti/Pt/Au pad metallization after AuSn reflow soldering tests using AuSn solder performs

Profilometer measurements on UEA: Measurements in the trenches of the UEA were performed to determine the height distribution of the glass structure between the spikes. The spikes of a UEA test chip were ground down to about 300 µm for laser profilometer measurements. For each linescan the distance between the highest glass peak and the other glass structures was calculated. Figure 4 depicts the linescan "Y03". The maximum difference on the analyzed UEA sample is 12.8 µm.

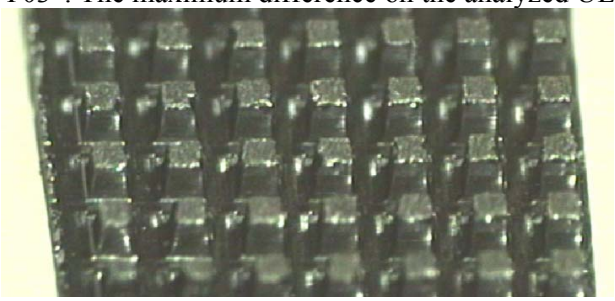

Fig. 13: light microscope image of the UEA after grinding

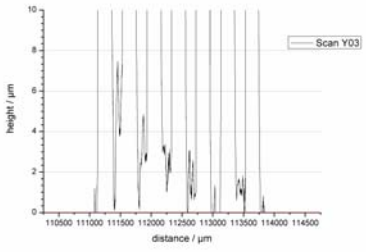

Fig. 14: Linescan "Y03"; the vertical lines are signals from the spikes.

Discussion/Interpretation of Results

The Ti/Pt/Au metallization showed excellent results after AuSn solder reflow testing. The selected metallization and the layer thicknesses can be used for the functional UEA chips. The profilometer measurements can be used for the final handling tool design and manufacturing.

Future Plans for Next Two (2) Quarters
First assembling tests using the UEA handling tools will give information about the maximum applicable stress and the heat transfer through the tool and the UEA during bonding. Both parameters (force and temperature) will influence the package bonding processes. The packaging concept for the integration of the coil and the SMD components will be further investigated based on the final IC and UEA design.

Subtask: handling tool
Description/ Rational
The substrate handling tool is designed for transportation and flip chip bonding of the UEA. The device has to function at high temperatures (>300 ^{0}C), show uniform thermal distribution, sustain compressive and thermal stresses during flip chip bonding and allow easy removal and placement of the UEA. A Si based design and fabrication process was selected due to the Si mechanical and thermal properties, as described in the first quarterly report. Pictures of the fabricated device are available upon request.

Experimental Results:
In order to verify the uniform thermal distribution and time taken for the substrate to heat up to the functional temperature Thermal images of the device were taken at its operating temperature at 300 ^{0}C and recorded over a period of 10 min.

Discussion/Interpretation of results:
Top and bottom features of the substrate holder were examined. Homogeneous etching of all patterned holes through the wafer was observed. The top hole diameter was 200 um, the hole pitch was 400 um. The thermal distribution across the substrate was obtained. The time required by the substrate to heat up to the required operating temperature can be predicted.

Future plans for the next (2) quarters
The substrate holder developed will be studied for long term use and their performance evaluated at higher operating temperatures. Stress due to thermal and mechanical stresses and the bond interface between the wafers will be examined.

Subtask: flip-chip test structures
Main Tasks Accomplished
The purpose of this subtask is to fabricate the under-bond metallization (UBM) layers for use in flip-chip bonding trials.

Description/Rationale
Initial trials for stud bumping of the Al UBM layers at IZM where unsuccessful do to the presence of a "tough layer" on the surface of the metallization. This tough layer prevented the solder from wetting the surface. Mitigation of the tough layer requires characterization of the layer composition and modification of the deposition and fabrication processes avoiding formation of this layer. Samples of diced and singulated 100 x 100 arrays where returned from IZM to the University of Utah, and SEM/EDX analysis was used to measure composition.

Experimental Results
A Hitachi S-3000 scanning electron microscope with EDAX brand EDX spectrometer was used. The information depth for EDX analysis is typically on the order of 1 µm with a primary beam potential of 20 kV, and decreases with lower accelerating voltages. EDX spectra where collected at 20, 10, and 5 kV in order to make the measurements increasingly surface sensitive at the lower voltages. This series of measurements allows an indirect evaluation of the surface composition of the Al UBM features in comparison with the "bulk" composition of the thin film. The compositions listed in table 3 were quantified from the respective EDX spectra using standard ZAF correction factors to account for the

changes in accelerating voltage. The large concentration of carbon in the metal layers is considered anomalous, so further analysis will be required to verify this result. Sources of carbon contamination in thin films often result from surface contamination of the sputtering target or contamination of the vacuum ambient by volatile hydrocarbons (pump oils, solvent vapors, photoresist).

Tab. 3: EDX measurements of Al metallization on flip-chip test wafer.

Accelerating Voltage (kV)	Carbon (at%)	Oxygen (at%)	Aluminum (at%)	Silicon (at%)
20	20.74%	2.95%	67.60%	8.72%
10	16.62%	2.94%	80.43%	0%
5	19.82%	5.06%	74.69%	0.43%

EDX measurements will be replicated in to verify the presence of the carbon content. If this is verified, the target composition itself will be measured to determine if it is contaminated. The residual gas analyzer mass spectrometer on the sputter deposition system will be used to monitor gas in the vacuum ambient. These steps should allow identification and mitigation of the contamination source. The oxygen concentration does not change between the 20 kV spectrum and the 10 kV spectrum. Easy interpretation is complicated by the presence of a significant Si concentration in the spectrum measured at 20 kV. This signal originates from the SiO_2 layer under the Al UBM layer. Because the SiO_2 substrate layer also contains oxygen, some of the oxygen concentration should be attributed to this layer, which suggests that the oxygen concentration in the Al layer should be lower. This indicated the presence of an oxide layer on the surface of the Al metal layer. The presence of this layer on the surface suggests that the oxidation is either occurring after the deposition process, or that the amount of oxygen in the vacuum ambient is increasing during the deposition process. Experience suggests that the former is the case, so a modified deposition and cool-down process will be used to avoid exposing the Al layer to room air at elevated temperatures. If this does not solve the problem, then the residual gas analyzer will also be used to monitor the vacuum ambient during the deposition run to investigate any changes in O_2 or H_2O partial pressures since these are the most common sources of oxygen contamination.

Future plans - following 2 quarters

The first priority will be improving the purity of the Al UBM layer to improve the solder wetting characteristics at the metal surface. This involves verifying the presence of carbon in the films, and if present, taking steps to decrease the carbon concentration. Also, to lower the oxygen concentration, the deposition process will be modified to allow the sputter deposited Al layer to cool down in a high-vacuum ($\sim 4x10^{-7}$ Torr) environment to mitigate surface oxidation. Once the contamination sources are mitigated, new test wafers will be produced for solder bumping and flip-chip bonding. These processes will then be precisely documented, and used for production of future test devices.

III.a.5 Task 5: Hermetic encapsulation and layer coating

III.a.5.1 SiC coating

Description/rationale

SiC coating is being carried out using Plasma Enhanced Chemical Vapor Deposition (PECVD). The key objective is to obtain highly dense, low stress SiC layers at low deposition temperatures (< 200 °C) to prevent damage to polymeric flip-chip underfiller materials as well as the parylene coating. Layer composition analysis is required to obtain high layer density, high resistivity, low defect density (surface micro-voids), and low dissolution rate in saline solution.

Experimental results

A stable process for SiC layer deposition with free Si and C content ratio was established. The deposition parameters we chose for amorphous hydrogenated-SiC were as follows: gas flow rate: methane: 9.5 sccm, silane: 4 sccm, hydrogen:74.5 sccm; substrate temperature : 280° C; RF power : 30 Watts; gas pressure : 400 mtorr; deposition time:2 hrs.

Discussion/Interpretation of results

EDX data shows an equivalent amount of C and Si which coincides with our expected film property. FT-IR data shows a large Si-C stretch band peak at wave number 780cm^{-1} further confirming our film composition to be SiC. The FT-IR also shows an oxide impurity peak, which needs to be eliminated.

Future plans for next two (2) quarters

We will further lower the deposition temperature for SiC. We will characterize the resistive and dielectric properties and perform accelerated aging test. The step coverage on the UEA geometry and adhesion of the layers will also be analyzed using SEM and a modified tape peel test.

III.a.5.2 Parylene coating

Description/ Rationale – adhesion/cohesion tests

A casting mold (Fig. 15) was developed and fabricated to insure a defined encapsulation area for hybrid layers (e.g Parylene and Silicone). For testing of the cohesion of the parylene film and the adhesion between the parylene layer and the corresponding substrate a tool for tensile strength tests was developed and fabricated (Fig. 16). The tool allows a simple investigation of the mechanical film properties regarding the adhesion on different rigid substrates (Peel Test) as well as investigations of different flexible substrates against each other (T-Peel Test).

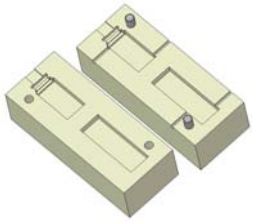

Fig. 15: Casting mold for sample preparation with different encapsulation materials (e.g. Silicone and Epoxy).

Fig. 16: Tool for tensile strength test of polymer films (Peel Tool).

Process optimization of the parylene C coating was performed. The dependance between the amount of the raw material (Dimer), the evaporation temperature and time and the process pressure was examined and recorded (Fig. 3). To optimize the process parameters and the properties of the parylene layer.

Experimental results

The results of the leakage current pretests showed a good handling of the probes as well as usable leakage current data. Encapsulations made with the casting mould were reproducible and showed a well defined shape. First peel test data on adhesion of parylene layers on different substrates appears very promising.

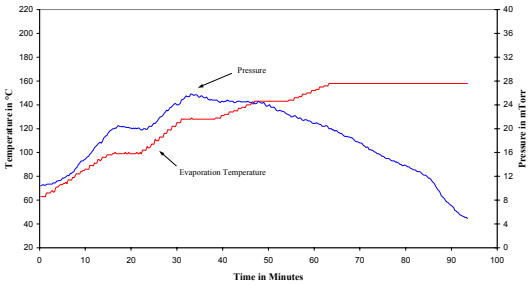

Fig. 17: Correlation between pressure and evaporation temperature of the parylene C coating process (12,5g dimer PPX-C).

Discussion / Interpretation of results

The casting mould yields well defined shapes. Several pretests showed the need of a minimum amount of probes to get useful statistical data. Test done with the peel test tool are very promising.

Future plans for the next (2) quarters

The leakage current test system will be optimized to increase the amount of testable probes. Several forms of adhesion tests are planned. First tests with the peel tool with parylene C on SiC and different subtrates

will be done. Different surface modifications to improve the adhesion of the polymer layer are intended as well as cohesion tests of the parylene layer itself.

Description and Rationale- electrical tests

Probes with eight Au interdigital structures (IDS) were patterned on 5 µm thick polyimide substrates with 300 nm thick Au metallization and a spacing of 200 µm. Pre-treated Teflon coated wires were soldered to the connector and to a carrier bottle lid. The probes were coated with 20 µm parylene C and immersed in 0.9% NaCl. The leakage current was measured at 5V DC bias voltage for 3 months at 37°C.

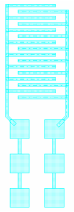

Fig. 18: Sample for leakage current test (Interdigital structure)

Results

Out of 4 probes monitored for 3 months, one probe failed (Fig. 19). The leakage current measured for the remaining probes was lass than one nA. On microscopic examination, the failure was found to be near the ceramic connector and not near the IDS, i.e. a short circuit of the conductive glue, which may have occurred during sample preparation.

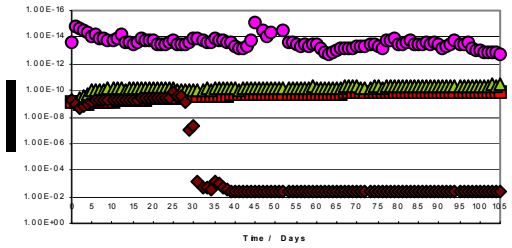

Fig. 19: Long term leakage tests; Parylene C (3 months, 37 °C.

Discussion / interpretation of results

The use of conductive glue found as a locus of failure so the test structures were modified by introducing microflex pads on the probes for connection to the ceramic plate. The initial test results also show pinhole freeness of parylene C coating. However, a high number of samples are being prepared to have statistical explanation.

III.a.5.3 double layer coating

n/a in second quarter, planned for third quarter

III.b.1 Task 6: Testing and validation of probe systems (in-vitro/in-vivo)

n/a at this stage of the project except for definition of test program

III.b.1.1 Bench testing of interface/electronics

n/a at this stage of the project

III.b.1.2 In-vivo testing of interface

No in-vivo testing at this stage of project

IV. Concerns

No major deviations or delays have occurred during the second quarter. We would however like to notify NIH/NINDS of one slight deviation from the original plan which from our current perspective does not impact the schedule and outcome of the project:

- Testing of the LTCC coils in the originally planned format has shown a fairly small safety margin to the minimum requirements in coupling and inductivity when making use of the screen printing technology currently employed to deposit the metal coils on the ceramic material. The limitations in aspect ratio and resolution of the technology used limit the number of turns, Q-factor and coupling coefficient of the coil. This could lead to unacceptably high voltages of the driving coil to induce sufficiently high voltages in the device to power the processor. In order to mitigate this risk, a telephone conference was initiated with partners IZM, IBMT and the University of Utah and a modification of the coil design proposed. The core concept prevails to make use of a) the frequency dependent shielding capability of the ferrite material protecting the signal processor from low frequency e-m fields powering the device while allowing transmission of the high frequency RF data signal and b) increased permeability and thus induction due to focusing of the field lines in the coil. In modification to the original approach however, a BCB base layer will be applied to the LTCC coil as basis for electroplated Au coils with 80 % bulk conductivity and 8 x 8 µm metallization cross section. This allows implementation of up to 100 windings and an increase in inductive coupling of about one order of magnitude. External driving voltages can thus be retained in a safe range of 24-100 V.

Salt Lake City, Utah, April 6th 2005

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